REMARKS

This paper responds to the Office Action mailed on February 23, 2005.

Claims 31 and 35 are amended. Claims 10-22, and 31-35 remain pending in this application.

Claim objections

Claims 31 and 35 were objected to because of the informalities.

Applicant amends claims 31 and 35 to correct the informalities as indicated in the Office Action.

§102 Rejection of the Claims

Claims 31 and 33 were rejected under 35 USC § 102(b) as being anticipated by Wood et al. (herein after Wood, U.S. 4,246,656).

Applicant respectfully traverses.

Independent claim 31 recites:

> "receiving a plurality of input bits at a plurality of input nodes of a plurality of register circuits;
> providing a plurality of output bits at a plurality of output nodes of the register circuits;
> performing a logic function on a plurality of bits held by the register circuits to produce a rotation number; and
> aligning a plurality of output bits provided at one of the output nodes with a plurality of output bits provided at other output nodes, based on the rotation number, when the plurality of input bits received at the input nodes are misaligned by at least one bit time interval."

Applicant is unable to find in Wood all of the things recited in claim 31. For example, Applicant is unable to find in Wood "performing a logic function on a plurality of bits held by the register circuits to produce a rotation number", and "aligning a plurality of output bits provided at one of the output nodes with a plurality of output bits provided at other output nodes, based on the rotation number, when the plurality of input bits received at the input nodes are misaligned by at least one bit time interval". Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 31.

Claim 33 indirectly depends on independent claim 31. Thus, claim 33 is also patentable over Wood for at least the reasons presented above regarding claim 31, plus the things recited in claim 33. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 33.

§103 Rejection of the Claims

Claim 10 was rejected under 35 USC § 103(a) as being unpatentable over Taya et al. (U.S. 5,778,214), hereafter Taya, in view of Yamamoto et al. (JP Publication 06-120937), hereafter Yamamoto.

Applicant respectfully traverses.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*
The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 24 USPQ2d 1443 (Fed. Cir. 1992). At the same time, however, although it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979)).

Applicant respectfully submits that the Office Action did not make out a *prima facie* case of obviousness for the following reasons:

Independent claim 10 recites:

"a plurality of input nodes;
a plurality of output nodes;
a plurality of register circuits, each of the register circuits being connected between one of the input nodes and one of the output nodes to receive a plurality of input bits at one of the input nodes and to provide at one of the output nodes a plurality of output bits based on the plurality of input bits;
a logic circuit connected to the register circuits to perform a logic function on the plurality of input bits held by one of the register circuits among the plurality of the register circuits with the plurality of input bits held by the other register circuits among the plurality of register circuits; and
a controller to configure the register circuits based on a result from the logic function of the logic circuit to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at one of the input nodes are misaligned with the plurality of input bits received at the other input nodes by one or more bit time intervals."

Applicant is unable to find in Taya all of the things recited in claim 10. For example, Applicant is unable to find in Taya "each of the register circuits being connected between one of the input nodes and one of the output nodes to receive a plurality of input bits at one of the input nodes and to provide at one of the output nodes a plurality of output bits based on the plurality of input bits".

Taya teaches, in FIG. 2, a plurality of shift registers 22a, 22b, and 22c. FIG. 2 of Taya shows that *all* of the input nodes of shift registers 22a, 22b, and 22c receive data from the same node (output node of SW 12a). In contrast, in claim 10, "each" of the register circuits being

connected between "one" of the input nodes and one of the output nodes to receive a plurality of input bits at "one" of the input nodes.

Further, Taya teaches, pattern check circuits 23a, 23b, and 23c (FIG. 2). Each of the pattern check circuit 23a, 23b, and 23c has an output node connected to a determination circuit 24. The Office Action compares the output node of each of the pattern check circuits 23a, 23b, and 23c of Taya to the output node of each of the register circuits of claim 10. However, the output node of each of the pattern check circuit 23a, 23b, and 23 of Taya provides a single pulse (see FIG. 3, 4, and 5). In contrast, in claim 10, the output of each of the register circuits provides "a plurality" of output bits. Thus, Applicant is unable to find in Taya a plurality of register circuits in which "each" of the register circuits is connected between one of the input nodes and one of the output nodes to receive a plurality of input bits at one of the input nodes and "to provide at one of the output nodes a plurality of output bits based on the plurality of input bits".

The Office Action combines a secondary reference (Yamamoto) with Taya to reject the logic circuit and the controller of claim 10. The Office Action states that Taya did not discuss the details of a logic circuit or a controller, as recited in claim 10. The Office Action further states that "it would have been obvious to one of ordinary skill in the art, having the teachings of Taya and Yamamoto before him at the time the invention was made, to modify the system taught by Taya to include the logic circuit and controller taught by Yamamoto, in order to obtain the claimed integrated circuit with simplicity and reduction in current consumption". Applicant respectfully disagrees.

The Office Action compares shift register 2 and storage means 4 of Yamamoto to the plurality of register circuits of claim 10. However, Applicant is unable to find in Yamamoto that each of the shift register 2 and storage means 4 of Yamamoto is connected between an input node and an output node to receive a plurality of input bits and to provide at the output node a plurality of output bits based on the plurality of input bits. In contrast, claim 10 recites, among other things, "a plurality of register circuits, each of the register circuits being connected between one of the input nodes and one of the output nodes to receive a plurality of input bits at one of the input nodes and to provide at one of the output nodes a plurality of output bits based on the plurality of input bits".

The Office Action further compares comparison means 3 of Yamamoto to the logic circuit of claim 10. However, Applicant is unable to find in Yamamoto details of the logic circuit as recited in claim 10. The Office Action states that comparison means 3 of Yamamoto performs a logic function on a bits held by shift register 2 with the bits held by storage means 4. Yamamoto shows storage means 4 being a single unit. Thus, comparison means 3 of Yamamoto performs a logic function on bits held by shift register 2 with another single unit or another single register (storage means 4). In contrast, the logic circuit of claim 10 performs a logic function on the bits held by one of the register circuits with the bits held by other register "circuits". The other register circuits are multiple circuits, whereas storage means 4 of Yamamoto is a single circuit. Thus, Applicant is unable to find in Yamamoto "a logic circuit connected to the register circuits to perform a logic function on the plurality of input bits held by one of the register circuits among the plurality of the register circuits with the plurality of input bits held by the other register circuits among the plurality of register circuits".

The Office Action further compares control means 5 of Yamamoto to the controller of claim 10. However, Applicant is unable to find in Yamamoto details of the controller as recited in claim 10. In Yamamoto, the purpose of control means 5 of Yamamoto is to shift one bit from shift register 1 to shift register 2 based on the comparison result from comparison means 3. Applicant is unable to find in Yamamoto a showing or a fair suggestion that the control means 5 of Yamamoto is used to configure both shift register 2 and storage means 4 based on the result from the comparison in comparison means 3 to align the bits at the output node of shift register 2 with the bits at the output node of storage means 4. In contrast, claim 10 recites that the controller of claim 10 is to "configure the register circuits based on a result from the logic function of the logic circuit to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at one of the input nodes are misaligned with the plurality of input bits received at the other input nodes by one or more bit time intervals".

Moreover, Applicant is unable to find in Taya and Yamamoto, either individual or in combination, a fair suggestion or motivation to combine Taya and Yamamoto, as proposed by the Office Action, to achieve the circuit recited in claim 10.

All of the reasons presented above show that a *prima facie* case of obviousness has not been made. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 10.

Claim 11 was rejected under 35 USC § 103(a) as being unpatentable over Taya et al. and Yamamoto et al. as applied to claim 10, and further in view of Fukuoka (U.S. 6,467,063).

Claim 11 depends on independent claim 10. As presented above, claim 10 is patentable over Taya and Yamamoto. Thus, claim 11 is also patentable over Taya and Yamamoto, and further over Fukuoka for at least the reasons presented above regarding claim 10, plus the things recited in claim 11. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 11.

Claims 12-13 were rejected under 35 USC § 103(a) as being unpatentable over Fukuoka, Taya, and Yamamoto as applied to claim 11 above, and further in view of Moriwaki et al. (U.S. 6,753,872).

Claims 12 and 13 indirectly depend on independent claim 10. As presented above, claim 10 is patentable over Taya and Yamamoto. Thus, claims 12 and 13 are also patentable over Fukuoka, Taya, Yamamoto, and further over Morikawi for at least the reasons presented above regarding claim 10, plus the things recited in claims 12 and 13. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claims 12 and 13.

Claims 14 and 16-17 were rejected under 35 USC § 103(a) as being unpatentable over Wood in view of Yamamoto and Fukuoka.

Applicant respectfully traverses because a case of *prima facie* case of obviousness has not been made.

Independent claim 14 recites:

> "a plurality of input nodes to receive a plurality of input bits;
> a plurality of output nodes to provide a plurality of output bits;
> a plurality of register circuits, each of the register circuits being connected between one of the input nodes and one of the output nodes, each of the register circuits including a number of register cells, the number of register cells equaled to 2M-1, where M is a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit, each of the register circuits further including a select circuit connected to a subset of the number of register cells through a number of select lines, the number of select lines

equaled to a maximum number of bit time intervals of misalignment of a parallel bus that connects to the integrated circuit;

a logic circuit connected to the register circuits to perform a logic function on a plurality of bits held by the register circuits, wherein the logic circuit includes:

a calculation unit to perform the logic function on a plurality of bits;

a plurality of memory units to store results from the logic function;

a counter to count values stored in the memory units;

a detect logic to determine results from the counter and to generate a rotation number, the rotation number being used to rotate data held in the number of register cells; and

a controller to configure the register circuits based on a result from the logic circuit to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at the input nodes are misaligned by one or more bit time intervals."

Applicant is unable to find in Wood all of the things recited in claim 14. For example, Applicant is unable to find in Wood "each of the register circuits further including a select circuit connected to a subset of the number of register cells through a number of select lines". Wood teaches a combination of 8-bit shift register 50 and 8-bit multiplexer 54 (FIG. 1). The Office Action compares this combination (8-bit shift register 50 and 8-bit multiplexer 54) of Wood to the register circuit of claim 14. However, as shown in FIG. 1 and as described in column 5 lines 2-12, the 8-bit multiplexer 54 of Wood is connected to all bits of the 8-bit shift register 50 through lines 62. In contrast, the selector circuit of claim 14 is connected to a "subset" of the register cells.

Moreover, Applicant is unable to find in Wood, Yamamoto, and Fukuoka, either individual or in combination, a fair suggestion or motivation to combine Wood, Yamamoto, and Fukuoka, as proposed by the Office Action, to achieve the circuit recited in claim 14.

All of the reasons presented above show that a *prima facie* case of obviousness has not been made. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 14.

Claims 16 and 17 depend on independent claim 14. As presented above, claim 14 is patentable over Wood, Yamamoto, and Fukuoka. Thus, claims 16 and 17 are also patentable over Wood, Yamamoto, and Fukuoka for at least the reasons presented above regarding claim 14, plus the things recited in claims 16 and 17. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claims 16 and 17.

Claim 15 was rejected under 35 USC § 103(a) as being unpatentable over Taya and Yamamoto as applied to claim 10 above, and further in view of Jaquette (U.S. 5,737,371).

Claim 15 depends on independent claim 10. As presented above, claim 10 is patentable over Taya and Yamamoto. Thus, claim 15 is also patentable over Taya and Yamamoto, and further over Jaquette for at least the reasons presented above regarding claim 10, plus the things recited in claim 15. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 15.

Claims 18-20 were rejected under 35 USC § 103(a) as being unpatentable over Moriwaki in view of Grondalski (U.S. 6,108,763) and Wood.

Applicant respectfully traverses because a *prima facie* case of obviousness has not been made.

Independent claim 18 recites:

"a parallel bus including a plurality of bus lines to carry a plurality of bits on each of the bus lines; and

a first integrated circuit including a plurality of register circuits, each of the register circuits being connected to one of the bus lines, and each of the register circuits including,

a shift register connected to an input node, the shift register including a plurality of register cells,

a select circuit connected to a subset of the number of register cells through a number of select lines, the select circuit including an output node, and

a controller connected to the select circuit and the register cells to configure the register cells to select only one of the select lines to be a part of a conductive path connected between the input node and the select circuit output node."

Moriwaki teaches a data transfer circuit 12 having a plurality of register circuits 50-1 through 50-64 (FIG. 5). Applicant is unable to find in Moriwaki a showing or a fair suggestion that "each" of the register circuits 50-1 through 50-64 of Moriwaki includes a shift register and a select circuit. Moriwaki shows a selector 51 (FIG. 5). However, selector 51 is the only selector used to select all of the register circuits 50-1 through 50-64 of Moriwaki. In contrast, claim 18 recites, among other things, a plurality of register circuits in which "each" of the register circuits includes a shift register and a select circuit.

Moreover, Applicant is unable to find in Moriwaki "a select circuit connected to a subset of the number of register cells through a number of select lines". Moriwaki teaches, in FIG. 5, a selector 51 connected to each of the register circuits 50-1 through 50-64 through select lines 24b

(24 bits). Column 9, lines 11 of Moriwaki states that each of the register circuits 50-1 through 50-64 has a capacity of 24 bits. Thus, selector 51 of Moriwaki is connected to all bits of each of the register circuits 50-1 through 50-64. In contrast, the selector circuit of claim 18 recites is connected to a "subset" of the register cells of each of the register circuits.

Regarding Wood, Applicant is unable to find in Wood "a select circuit connected to a subset of the number of register cells through a number of select lines". Wood teaches, in FIG. 1, a combination of 8-bit shift register 50 and 8-bit multiplexer 54. The Office Action compares this combination (8-bit shift register 50 and 8-bit multiplexer 54) of Wood to the register circuit of claim 18. However, as shown in FIG. 1 and as described column 5 lines 2-12, the 8-bit multiplexer 54 of Wood is connected to all bits of the 8-bit shift register 50 through lines 62. In contrast, the selector circuit of claim 18 is connected to a "subset" of the register cells of each of the register circuits.

Further, Applicant is unable to find in Moriwaki, Grondalski, and Wood, either individual or in combination, a fair suggestion or motivation to combine Moriwaki, Grondalski, and Wood, as proposed by the Office Action, to achieve the system recited in claim 18.

All of the reasons presented above show that a *prima facie* case of obviousness has not been made. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 10.

Claims 19 and 20 depend on independent claim 18. As presented above, claim 18 is patentable over Moriwaki, Grondalski, and Wood. Thus, claims 19 and 20 are also patentable over Moriwaki, Grondalski, and Wood for at least the reasons presented above regarding claim 18, plus the things recited in claims 19 and 20. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claims 19 and 20.

Claim 21 was rejected under 35 USC § 103(a) as being unpatentable over Wood, Moriwaki, and Grondalski as applied to claim 19 above, and further in view of Barnsley et al. (U.S. 5,430,812).

Applicant respectfully traverses because a *prima facie* case of obviousness has not been made.

Claim 21 indirectly depends on independent claim 18. As presented above, claim 18 is patentable over Moriwaki, Grondalski, and Wood. Thus, claim 21 is also patentable over Wood, Moriwaki, and Grondalski and further over Barnsley for at least the reasons presented above

regarding claim 18, plus the things recited in claim 21. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 21.

Claim 22 was rejected under 35 USC § 103(a) as being unpatentable over Wood, Moriwaki, and Grondalski as applied to claim 19 above and further in view of Frisch et al. (U.S. 4,707,834).

Applicant respectfully traverses because a *prima facie* case of obviousness has not been made.

Claim 22 indirectly depends on independent claim 18. As presented above, claim 18 is patentable over Moriwaki, Grondalski, and Wood. Thus, claim 22 is also patentable over Wood, Moriwaki, and Grondalski and further over Barnsley for at least the reasons presented above regarding claim 18, plus the things recited in claim 22. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 22.

Claims 32 and 34 were rejected under 35 USC § 103(a) as being unpatentable over Wood as applied to claim 31 above, and further in view of Fukuoka.

Claim 32 depends on independent claim 31. As presented above, claim 31 is patentable over Wood. Thus, claim 32 is also patentable over Wood and further in view of Fukuoka for at least the reasons presented above regarding claim 31, plus the things recited in claim 32. Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 32.

Claim 34 indirectly depends on independent claim 31. As presented above, claim 31 is patentable over Wood. Thus, claim 34 is also patentable over Wood and further in view of Fukuoka for at least the reasons presented above regarding claim 31, plus the things recited in claim 34 Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 34.

Claim 35 was rejected under 35 USC § 103(a) as being unpatentable over Wood as applied to claim 31 above, and further in view of Yamamoto.

Claim 35 depends on independent claim 31. As presented above, claim 31 is patentable over Wood. Thus, claim 35 is also patentable over Wood and further in view of Yamamoto for at least the reasons presented above regarding claim 31, plus the things recited in claim 35 Accordingly, Applicant requests reconsideration and withdrawal of the rejection, and allowance of claim 35.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6969) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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